speed of operations depends, among many things including, for example, the clock cycle time, and the clock cycle time, in turn is dependent on the amount of logic between any two pipeline stages. The smaller the amount of logic between the pipeline registers, the faster can the clock can be, thereby improving throughput. However, spreading the logic too thin will lead to a large number of pipe stages where the initial latency will be quite long.

In The Drawings

Please replace Figure 1 as filed with attached Figure 1.

Remarks

The correction to the Specification is rendered for grammatical accuracy. Replacement Figure 1 adds no new matter, and is described in the Specification; for example pages 6, lines 26-29 and page 7, lines 1-10.

A favorable reply is earnestly requested.

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Attachments: Figure 1; Specification Revision page

Serial No. 10/005,551

The above specification changes are reflected below, with underlines showing inserts and brackets showing deletions.

At page 6-7, lines 26-29 and 1-10, the changes are as follows:

Another important aspect and application of the present invention is illustrated in FIG. 1 by way of a digital filtering circuit 100. The datapath unit 102 is a pipelined cascade of combinational logic circuits 110a, 110b, and including arithmetic operations such as additions, subtractions, multiplications, and/or logical operations such as AND, OR, NOT, MULTIPLEX, SHIFT. After each combinational logic circuit, a pipelined register 112a, 112b, etc. is used to feed the result of the previously-executing combinational logic circuit to the next combinational logic circuit. The datapath 102 is controlled by the control/mode processor 120 with data [is] being fed through memory 130 for processing by the pipelined datapath unit 102 and sent out. The speed of operations depends, among many things including, for example, the clock cycle time, and the clock cycle time, in turn is dependent on the amount of logic between any two pipeline stages. The smaller the amount of logic between the pipeline registers, the faster can the clock can be, thereby improving throughput. However, spreading the logic too thin will lead to a large number of pipe stages where the initial latency will be quite long.

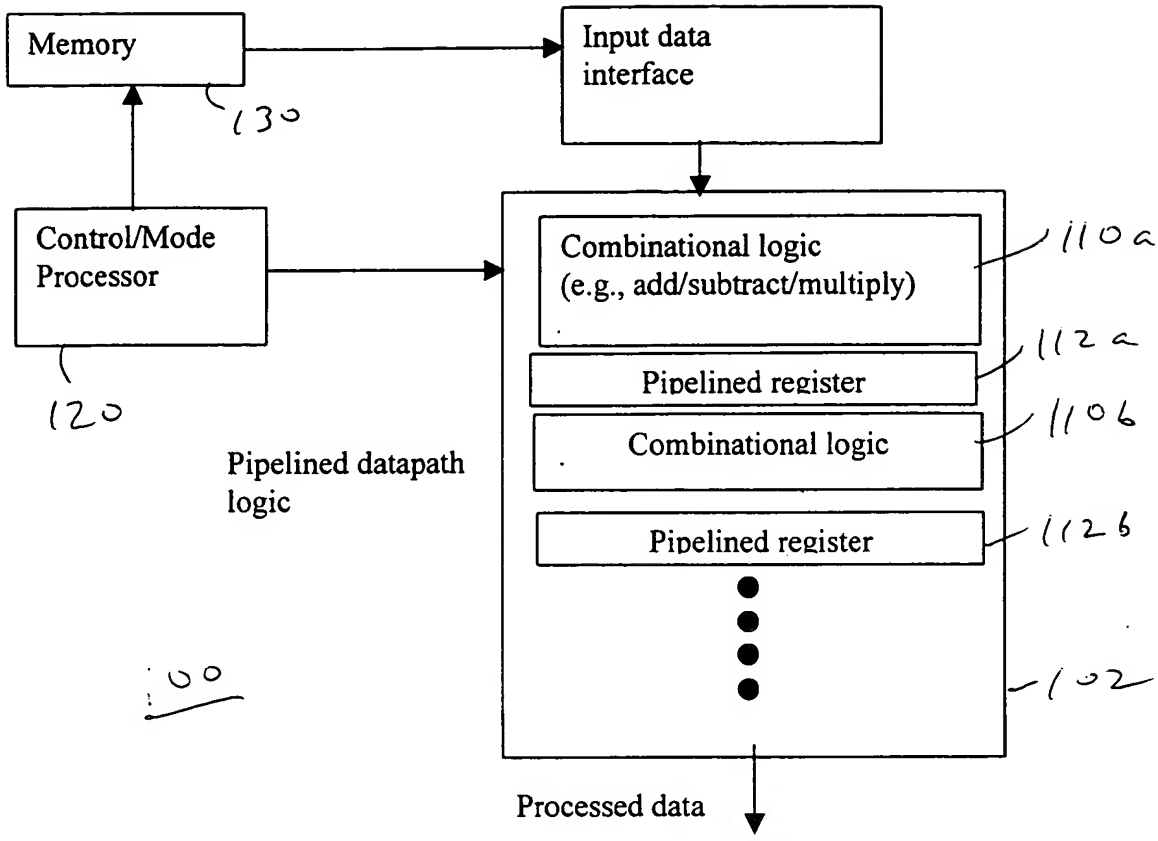
Memory
130
Input data interface
Control/Mode Processor
120
Combinational logic (e.g., add/subtract/multiply)
110a
Pipelined register
112a
Combinational logic
110b
Pipelined register
112b
Pipelined datapath logic
100
102
Processed data

FIG. 1